

Data sheet acquired from Harris Semiconductor SCHS119

# CD54HC245, CD54HCT245, CD74HC245, CD74HCT245

High Speed CMOS Logic Octal-Bus Transceiver, Three-State, Non-Inverting

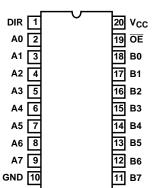
November 1997

#### **Features**

- · Buffered Inputs
- Three-State Outputs
- . Bus Line Driving Capability
- Typical Propagation Delay (A to B, B to A) 9ns at V<sub>CC</sub> = 5V, C<sub>L</sub> = 15pF, T<sub>A</sub> = 25°C
- Fanout (Over Temperature Range)
  - Standard Outputs........... 10 LSTTL Loads
  - Bus Driver Outputs ...... 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N<sub>IL</sub> = 30%, N<sub>IH</sub> = 30% of V<sub>CC</sub> at V<sub>CC</sub> = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,
     V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility, I<sub>I</sub>  $\leq$  1 $\mu$ A at V<sub>OL</sub>, V<sub>OH</sub>

#### **Pinout**

CD54HC245, CD54HCT245, CD74HCT245 (CERDIP, PDIP, SOIC) TOP VIEW



#### Description

The Harris CD54HC245, CD54HCT245, and CD74HC245, CD74HCT245 are high-speed octal three-state bidirectional transceivers intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation while driving large bus capacitances. They provide the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LSTTL circuits.

The CD54HC245, CD54HCT245, CD74HC245 and CD74HCT245 allow data transmission of the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input ( $\overline{\text{OE}}$ ), when high, puts the I/O ports in the high-impedance state

The HC/HCT245 is similar in operation to the HC/HCT640

and the HC/HCT643.

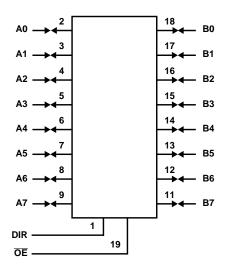
## **Ordering Information**

PART NUMBER	TEMP. RANGE ( <sup>O</sup> C)	PACKAGE	PKG. NO.
CD54HC245F	-55 to 125	20 Ld CERDIP	F20.3
CD54HCT245F	-55 to 125	20 Ld CERDIP	F20.3
CD74HC245E	-55 to 125	20 Ld PDIP	E20.3
CD74HCT245E	-55 to 125	20 Ld PDIP	E20.3
CD74HC245M	-55 to 125	20 Ld SOIC	M20.3
CD74HCT245M	-55 to 125	20 Ld SOIC	M20.3

#### NOTES:

- 1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
- Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

#### Functional Diagram



#### TRUTH TABLE

CONTROL INPUTS		
ŌĒ	DIR	OPERATION
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	Х	Isolation

H = High Level, L = Low Level, X = Irrelevant To prevent excess currents in the High-Z (Isolation) modes all I/O terminals should be terminated with 10k $\Omega$  to 1M $\Omega$  resistors.

## **Absolute Maximum Ratings**

DC Supply Voltage, V <sub>CC</sub> 0.5V to 7V
DC Input Diode Current, I <sub>IK</sub>
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ ±20mA
DC Output Diode Current, I <sub>OK</sub>
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ ±20mA
DC Drain Current, per Output, IO
For $-0.5V < V_O < V_{CC} + 0.5V$ ±35mA
DC Output Source or Sink Current per Output Pin, IO
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$
DC $V_{CC}$ or Ground Current, $I_{CC}$

#### **Thermal Information**

Thermal Resistance (Typical, Note 3) $\theta_{JA}$	Y (oc/M	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	125	N/A
SOIC Package	120	N/A
CERDIP Package	100	40
Maximum Junction Temperature		150 <sup>o</sup> C
Maximum Storage Temperature Range		-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)		300°C
(SOIC - Lead Tips Only)		

### **Operating Conditions**

Temperature Range, $T_A$ 55 $^{0}$ C to 125 $^{0}$ C Supply Voltage Range, $V_{CC}$
HC Types2V to 6V
HCT Types
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub> 0V to V <sub>CC</sub>
Input Rise and Fall Time
2V
4.5V
6V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

3.  $\theta_{\mbox{\scriptsize JA}}$  is measured with the component mounted on an evaluation PC board in free air.

## **DC Electrical Specifications**

		TE: CONDI				25 <sup>0</sup> C			O 85°C	-55°C TO 125°C				
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS		
HC TYPES														
High Level Input	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output	VoH	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
Voltage CMOS Loads			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
Omeo Edudo						-0.02	6	5.9	-	-	5.9	-	5.9	-
High Level Output	7		-	-	-	-	-	-	-	-	-	V		
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V		
112 20000			-5.2	6	5.48	-	-	5.34	-	5.2	-	V		
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
Voltage CMOS Loads			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
OWOO Loads			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads	7		-	-	-	-	-	-	-	-	-	V		
			4	4.5	-	-	0.26	-	0.33	-	0.4	V		
			5.2	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	II	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μА		

# DC Electrical Specifications (Continued)

		TE: CONDI		V <sub>CC</sub>		25°C		-40°C 1	O 85°C	-55°C T	O 125°C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	8	-	80	-	160	μΑ
Three-State Leakage Current	l <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5	-	±10	μА
HCT TYPES	•	•	•			•	•	•				
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μА
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μА
Three-State Leakage Current	l <sub>OZ</sub>	V <sub>IL</sub> or V <sub>IH</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	6	-	-	±0.5	-	±5	-	±10	μА
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	Δl <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μА

NOTE: For dual-supply systems theoretical worst case ( $V_I$  = 2.4V,  $V_{CC}$  = 5.5V) specification is 1.8mA.

## **HCT Input Loading Table**

INPUT	UNIT LOADS
An or Bn	0.4
ŌĒ	1.5
DIR	0.9

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Table, e.g., 360µA max at  $25^{o}C.$ 

# **Switching Specifications** $C_L = 50pF$ , Input $t_r$ , $t_f = 6ns$

		TEST		25°C			-40°C TO 85°C		-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
HC TYPES											
Propagation Delay Data to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	110	-	140	-	165	ns
			4.5	-	-	22	-	28	-	33	ns
		C <sub>L</sub> = 15pF	5	-	9	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	19	-	24	-	28	ns
Output Disable to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C <sub>L</sub> = 15pF	5	-	12	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	26	-	33	-	38	ns
Output Enable to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
		C <sub>L</sub> = 15pF	5	-	12	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	26	-	33	-	38	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	2	-	-	60	-	75	-	90	ns
			4.5	-	-	12	-	15	-	18	ns
			6	-	-	10	-	13	-	15	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	C <sub>O</sub>	-	-	-	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C <sub>PD</sub>	-	5	-	53	-	-	-	-	-	pF
HCT TYPES	I		<u> </u>							<u>!</u>	
Propagation Delay Data to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	26	-	33	-	39	ns
	·	C <sub>L</sub> = 15pF	5	-	10	-	-	-	-	-	ns
Output Disable to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	30	-	38	-	45	ns
		C <sub>L</sub> = 15pF	5	-	12	-	-	-	-	-	ns
Output Enable to Output	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	32	-	40	-	48	ns
		C <sub>L</sub> = 15pF	5	-	13	-	-	-	-	-	ns
Output Transition Time	t <sub>THL</sub> , t <sub>TLH</sub>	C <sub>L</sub> = 50pF	4.5	-	-	12	-	15	-	18	ns
Input Capacitance	C <sub>IN</sub>	C <sub>L</sub> = 50pF	-	10	-	10	-	10	-	10	pF
Three-State Output Capacitance	CO	-	-	-	-	20	-	20	-	20	pF
Power Dissipation Capacitance (Notes 4, 5)	C <sub>PD</sub>	-	5	-	55	-	-	-	-	-	pF

## NOTES:

- 4.  $C_{\mbox{\scriptsize PD}}$  is used to determine the dynamic power consumption, per channel.
- 5.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

#### Test Circuits and Waveforms

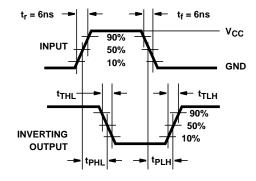


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

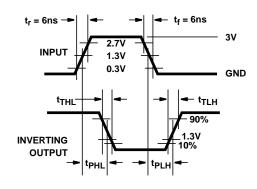


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

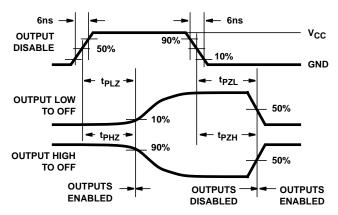


FIGURE 3. HC THREE-STATE PROPAGATION DELAY WAVEFORM

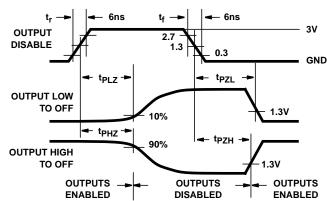
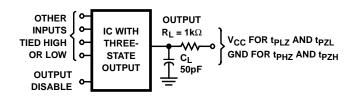


FIGURE 4. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 5. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

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